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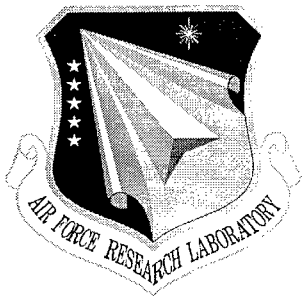

CLASSICAL COMBINATORIAL AND SEQUENTIAL MACHINE COMPONENTS IMPLEMENTED WITH QUANTUM DEVICES

Syracuse University

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APPROVED:

STEVEN P. HOTALING
Project Engineer

FOR THE DIRECTOR:

ROBERT G. POLCE, Acting Chief
Rome Operations Office
Sensors Directorate

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CLASSICAL COMBINATORIAL AND SEQUENTIAL MACHINE COMPONENTS IMPLEMENTED WITH QUANTUM DEVICES

Daniel J. Pease

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Principal Investigator: Daniel J. Pease
Phone: (315) 443-4418

AFRL Project Engineer: Steven P. Hotaling
Phone: (315) 330-2487

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Daniel J. Pease

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Syracuse University
Office of Sponsored Programs
113 Bowne Hall
Syracuse NY 13244-1200

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The majority of work today relating to quantum computing has provided results that are almost incomprehensible to even the most advanced computer architect. This paper uses the recent research results of quantum mechanical logic as building blocks to derive a computer architecture based on quantum devices that is consistent with existing system architectures. The new and admittedly exotic nature of quantum computing notwithstanding, this work presents a quantum mechanical analog of a finite state machine which may be realized from a present day architectural framework. Existing architectures are finite state sequential machines with binary data representations, asynchronous combinatorial Boolean logic and synchronous memory. Synchronous combinatorial logic with a binary data representation and implementations of D, T and JK flip-flops, which are the primary forms of synchrouous memory, are presented using quantum and near quantum devices. Even the issue of reliable operation of quantum devices is addressed by suggesting that redundancy and quantum majority logic could perform single error correction at key points within the quantum system. Quantum devices can be a step in the evolution of advanced computer architectures.

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Abstract

The majority of work today relating to quantum computing has provided results that are almost incomprehensible to even the most advanced computer architect. This paper uses the recent research results of quantum mechanical logic as building blocks to derive a computer architecture based on quantum devices that is consistent with existing system architectures.

The new and admittedly exotic nature of quantum computing notwithstanding, this work presents a quantum mechanical analog of a finite state machine which may be realized from a present day architectural framework. Existing architectures are finite state sequential machines with binary data representations, asynchronous combinatorial Boolean logic, and synchronous memory. Synchronous combinatorial logic with a binary data representation and implementations of D, T and JK flip-flops, which are the primary forms of synchronous memory, are presented using quantum and near quantum devices. Even the issue of reliable operation of quantum devices is addressed by suggesting that redundancy and quantum majority logic could perform single error correction at key points within the quantum system. Quantum devices can be a step in the evolution of advanced computer architectures.

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There have been some significant advancements recently in the technical literature about quantum computing. From a computer architect's perspective, quantum computer development at the present time seems to be aimed at revolutionary concepts including: atomic devices which demonstrate the viability of quantum devices, reversible quantum logic, devices with radix-R data representations, and special applications that will benefit from quantum systems. The papers are complex, elegant works that are leading off in many interesting directions. As a whole they make the quantum computer seem very exotic. This is also a problem, because they also seem to be quantum computational scientific wanderings leading to systems with very limited application. Exotic architectures of the past have not been widely accepted or significant commercial successes. If quantum computing is going to become the computer architecture of the future, well ordered evolution is needed that can be widely understood and applied.

This paper takes recent quantum developments and attempts to identify what is needed to connect them to the present state of computer components. All computer systems are finite state sequential machines. These are made up of combinatorial components implementing Boolean expressions and fundamental memory devices used to store state. The author believes quantum devices can be used to implement combinatorial and memory devices that will be consistent with existing system architectures. Multi-level, multiple-output combinatorial logic gate structures can be implemented with quantum devices. These have to be operated synchronously, rather than asynchronously, but the logic functions can be implemented. All the basic memory devices: latch, D flip-flop, T flip-flop, and JK flip-flop can be implemented with quantum devices. These have to be clocked at quantum speeds, rather than existing clock rates, but they do provide memory that is the basis of all sequential machines.

Continuing effort should be made in the exotic quantum development areas. They offer some potentially exciting new computational capabilities; But there should also be some efforts at

evolving from present day architectures to quantum computers performing like existing systems. Its time for some quantum computational engineering.

Choosing a Data Model for Quantum Computing

Bennett, Bernstein, Brassard, and Vazirani [3] have suggested that a quantum computer will be a very special and unique device, performing certain important functions very effectively. Many recent publications have suggested application areas where quantum systems offer significant application:

- Cryptography: Barenco, Deutsch, and Ekert [2], Brandt [6], Brassard [7], Coppersmith [11], and Shor [26].
- Large System Modeling: Cirac and Zoller [10], Feynman [14], Knill [18], Simon [27], and Zapatrin [29].
- Large Scale Real-Time Processing: Chuang [9], Filnov and Wigner [15], and Hogg [16]

They have also suggested that quantum devices have some very unique and interesting properties:

- Using radix-k rather than binary: Hotaling [17]
- Systolic operation: Margolus [21]
- Reversible logic functions: Bennett [4], Bose [5], Cory [12], Konstantin [20], Toffoli [28]
- Universal logic gates: Barenco [1], DiVincenzo [13], and Mozyrsky [21-23]

These are all very interesting and should be studied in great depth. But, it is the author's belief that for quantum logic to be truly successful, it has to be able to operate in the existing Boolean based sequential machine model of operation. This paper is aimed at looking at this issue.

To implement the existing model of computation, a quantum system would have to meet the following model:

(1) Basic information representation is in binary.

(2) Basic operations are AND, OR, and NOT, or some other functionally complete Boolean algebra.

(3) Be able to operate synchronously.

(4) Be able to operate asynchronously through many levels of logic.

(5) Provide a bistable memory device.

(6) Interface with existing devices.

The first two capabilities have been shown in recent papers by Barenco [2] and DiVincenzo [13]. The Tofolli universal logic gate has been shown to, with proper control inputs, be able to implement functionally complete base two Boolean logic. There are some serious limitations of quantum logic devices that make the implementation of the remaining capabilities of the present data model of computation challenging. These limitations are:

(1) The quantum devices are only stable for a short period of time.

(2) When the output of a quantum device is read it destroys the value held by the device.

(3) If quantum devices get too large, they become a molecule and do not behave as true quantum logic devices.

(4) Quantum device operation is not as inherently reliable (as will be defined later) as existing logic technology.

This paper will now try to suggest some ideas that may make quantum logic devices able to implement existing logic structures even within the limitations mentioned above.

The solutions suggested in this paper are:

(1) Using synchronous control of quantum read/write elements, a multilevel asynchronous logic structure can be implemented. All combinatorial logic can be implemented using two levels of logic. Strict rules for two-level Product-of-Sums and Sum-of-Product implementations are used in logic design. Cost optimization results in more levels, but fewer gates and inputs. Gate arrays and programmable logic are now widely used and are themselves multilevel. Quantum systems have to be able to implement all two-level and multilevel logic circuits.

(2) Use of quantum delay elements for signals in many layered structures to solve the limitation on stability of quantum devices.

(3) Create a quantum latch from delay devices that implement memory capabilities.

(4) Show that D, T and JK flip-flop, which are the basis of synchronous machine structures, can be implemented with quantum devices.

(5) Show how majority logic can be used to link redundant logic structures to increase the reliability of quantum device operation.

Quantum Implementation of Multilevel Combinatorial Logic

The basis of multilevel combinatorial quantum logic will be implemented using reader/writer. It will detect (Read) an output of another quantum device as a zero or a one, and then provide (Write) the value to the input of a different quantum device.

The reader/writer element is shown in Figure 1.

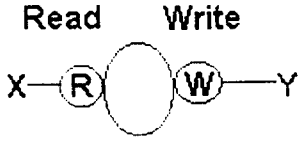

Figure 1. Quantum Reader/Writer
Reads value on X as a 0 or 1 and then writes value to Y.

This reader/writer will be used for three purposes:

(1) To provide isolation between the different quantum devices making up the logic structure. The reader/writer will isolate them from one another so they do not grow too large and become molecules.

(2) They will provide a point of synchronization. A set of reader/writers activated at the same time implement the transference of the results for one level of logic to the next level of logic.

(3) To provide a more reliable movement of one's and zeros through the logic structure, since it will read and pass a one or zero even if there is small variations in the value being read.

The reader/writers will be active only to transfer information between the logic gates. When it is not active, it will separate the operation of the logic gates themselves. Activating all of the reader/writers on one level of a logic structure at the same time will be done soon enough so that the result of one level is passed on before it becomes unstable.

Finally, the reader/writer is used because it will detect a zero or a one, depending on the spin of the device being read. This result will be detected even if there is some variation in the energy and operation of the logic device due to unreliability. The unreliability will be reduced because many close but different energy levels all will be considered a one and another seat will be considered a zero. The reader/writer will always give a one or zero result. There will be no indeterminate state which can occur in existing transistor based logic.

An example of a conventional multi-level logic implementation is shown in Figure 2.

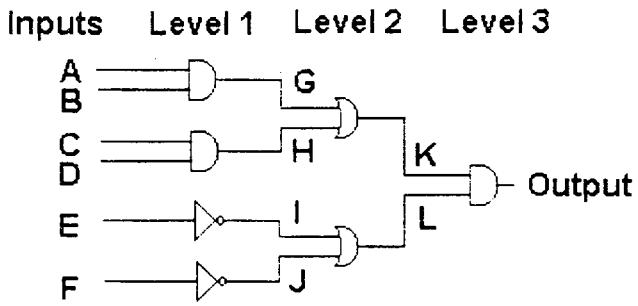

Figure 2. Multi-Level Logic Circuit

The inputs (A-F) are presented to the first level of inverters and gates. Depending on the switching times of those gates, outputs (G-I) will stabilize at different times. These partial results (G-I) will then pass through the OR gates on the second level and after a switching delay for the OR gates, the partial results K and L will stabilize. Then the final AND gate will switch based on K and L and the circuit's output will be correct and stable.

This circuit operates asynchronously and the output is not valid until all of the gates have switched, based on inputs derived from the initial inputs to level one. No clocking or control is used in this combinatorial circuit.

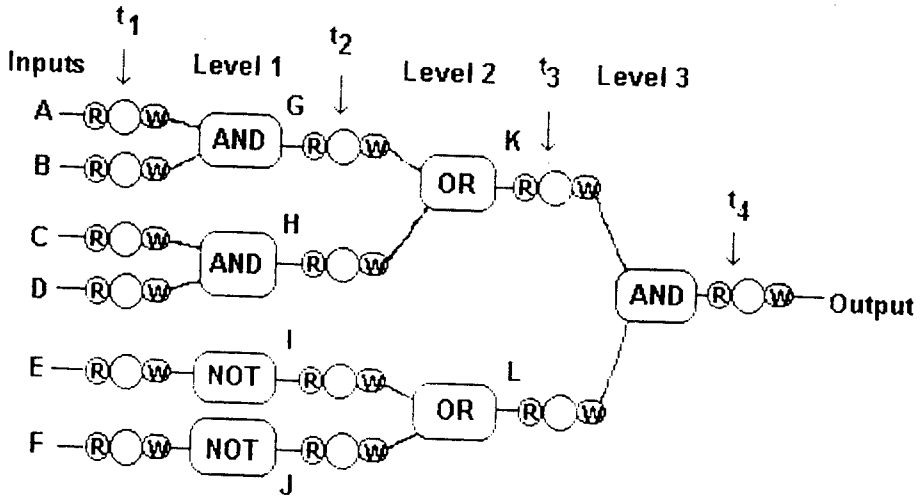

Figure 3. Multi-Level Circuit Implemented with Quantum Devices

Figure 3 shows how this could be implemented using quantum reader/writers at the inputs, between levels, and at the output. The gates are Tofolli quantum gates, and only the logic inputs and outputs are shown. The circuit operates unidirectionally from left to right.

All the six reader/writers are connected between the inputs and logic gates in level one and are activated at the same time (t_1). The second group of reader/writers is activated at t_2 so the logic gates function properly and soon enough to maximize the stability at the values on the output of the gates. It should be noted that when the gates on level 1 are read, all of the information in them is corrupted. This is acceptable because the reader/writers have passed the results of level one gate outputs on to the inputs of the gates at level 2. At time t_3, the outputs of level 2 gates are read and written into the inputs of the gate at level 3. Finally, at time t_4, the output of the last gate is read. This output is only valid during this read.

A timing diagram showing this operation is shown in figure 4.

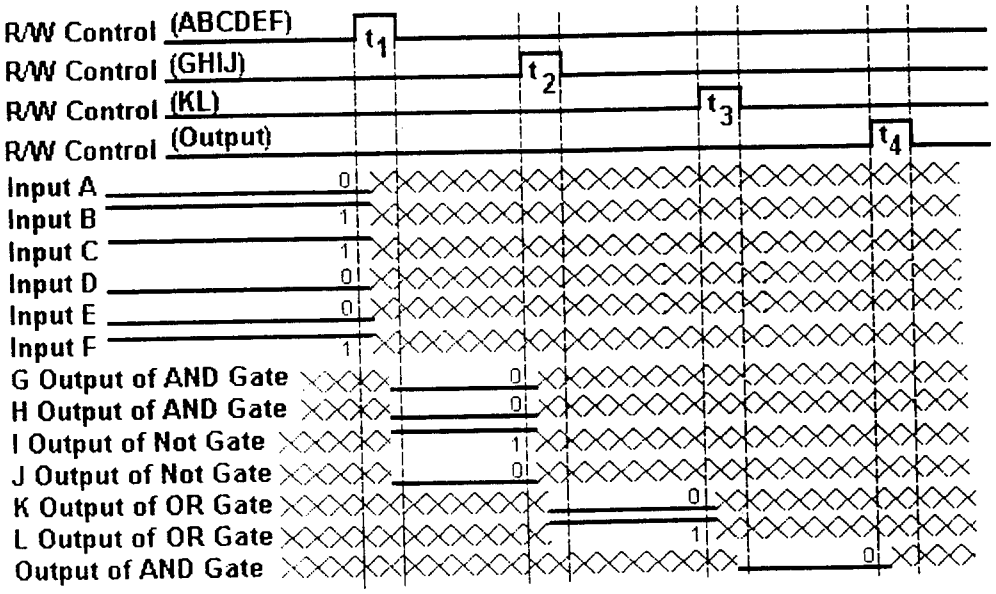

Figure 4 Timing Diagram for a Multi-Level Quantum System

In the timing diagram, note the six inputs are read at the same time with the six reader/writers. The quantum circuit will operate like the transistor-based circuit, but each level will have to be activated by pulsing the set of read/writers as shown. The quantum circuit will implement the asynchronous circuit. The only difference will be that the quantum circuit will be run synchronously, and the output will only be available when the output reader/writer is activated. If it is necessary to hold this result for some length of time a quantum latch (discussed at a later time) could be used.

Systolic Multilevel Operation

An interesting aside can be noted at this point. In the quantum circuit a new set of inputs could be presented at time t_2, and this will cause the input levels to start to process the result before the output has been obtained. An example of the timing diagram for this systolic operation

is shown in Figure 5. Note in Figure 5 the change of inputs after two cycles and the resultant change of outputs in the bottom row. This is quite different from existing device technology. New inputs cannot be presented to the circuit until the output has stabilized and been used.

The reason to have to wait until t_2 is that the read is destructive and destabilizes the operation of the gate. So, in order to guarantee that a gate isn't being written and read at the same time, an extra cycle is waited. The result is that the quantum circuit could be operated in a systolic manner with all even level reader/writers being active at the same time, and all the odd level reader/writers being active on the next cycle. This systolic pipelined operation has a performance advantage over existing technology.

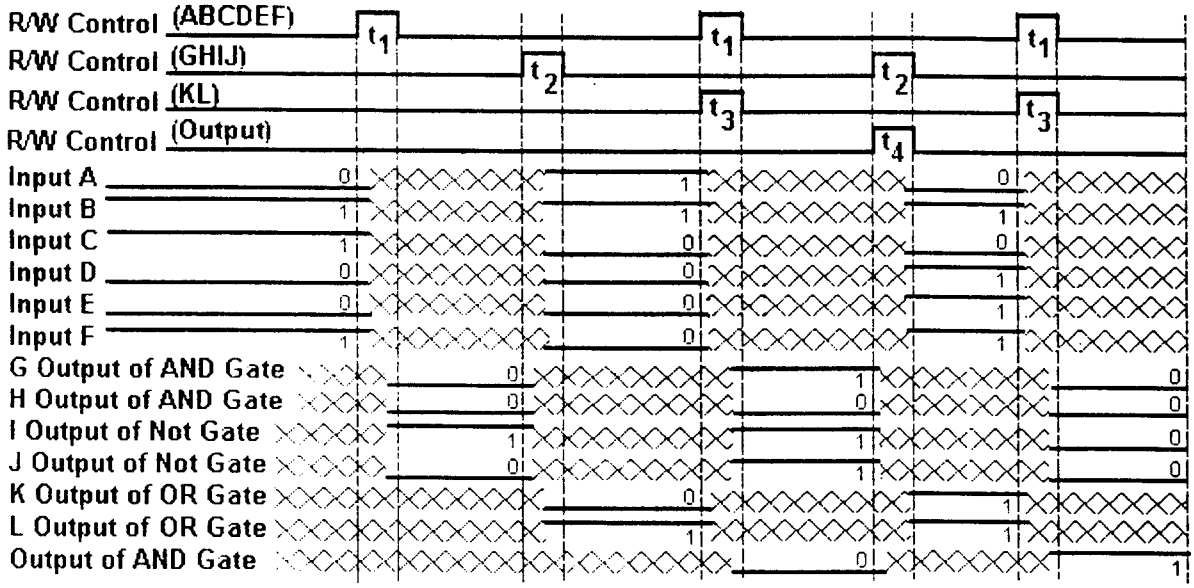

Figure 5 Timing Diagram for Systolic Operation of the Example Quantum Logic Circuit

Multi-level Logic with Inputs at Several Levels

There is an interesting problem for quantum implementations of multi-level logic. Inputs can be made at different levels. This isn't a problem for transistor based circuits because they operate asynchronously. In a quantum circuit, inputs are not held statically awaiting a levels outputs to stabilize.

An example of a conventional circuit is shown in Figure 6.

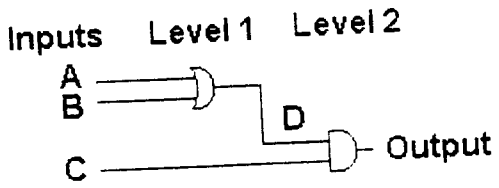

Figure 6. Multi-Level Logic System with Inputs at Different Levels

The inputs A. B and C are presented at the same time to the circuit. Inputs A and B cause the OR gate on Level 1 to switch. When its output (D) stabilizes, it and the input C will cause the AND gate on level two to switch. Then the output will stabilize.

In a quantum circuit, the input C to the AND gate will not be available and stable since it has to wait for the OR gate to operate on the inputs A and B. This problem will be solved by introducing a small dynamic bit storage element called a quantum delay gate. This is shown in Figure 7 and will be a 4 atom gate which can be written to by either of the two input reader/writers and read from by either or both reader/writers.

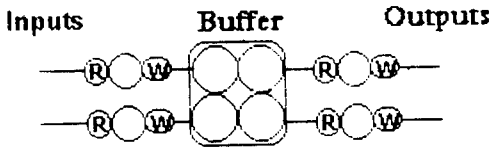

Figure 7.Qunatum Delay Element A four atom device which will store the value read by one of the reader/writer inputs and can output the stored value to both output reader/writer elements.

Its purpose is to hold a value while quantum logic gates at one level are performing their functions. Using this delay element is necessary because it will put the input value at the right level at the correct time. A four atom delay cell was used so it could be used later on in the memory ring. It is the smallest and therefore most reliable structure needed to perform the bit storage for a single cycle.

Using this quantum delay element, the multilevel logic structure shown in figure 6 can be implemented with quantum logic devices. This is shown in figure 8.

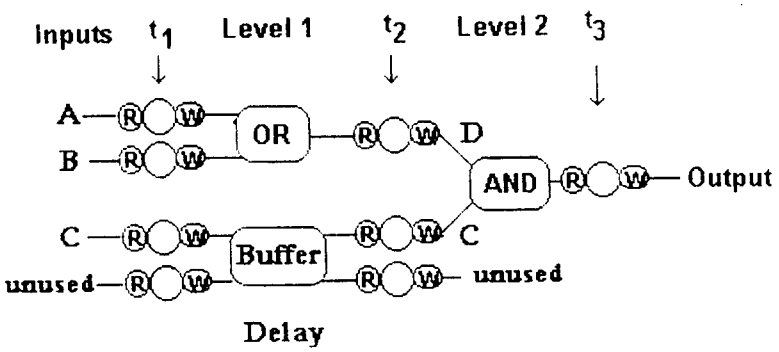

Figure 8 Quantum Implementation of Multi-Level Logic with Inputs at Different Levels

The input C is stored in the quantum delay gate at level 1 while the quantum OR gate processes the inputs A and B. The output of the OR, D, and the output of the delay gate, C, are then synchronously input to the AND gate. The timing diagram for this quantum circuit is shown in Figure 9.

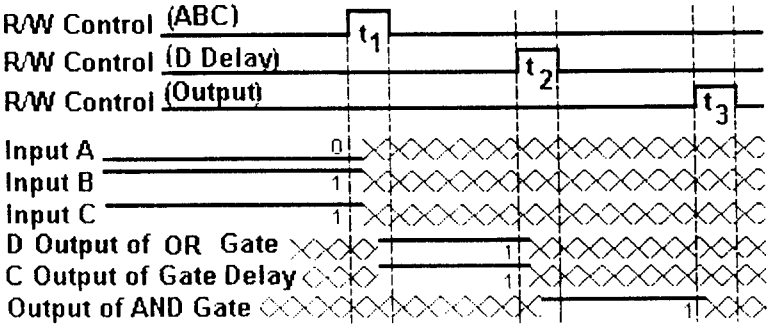

Figure 9 Timing Diagram for Quantum Multi-Level Logic with Inputs at Different Levels

Note the values of C being held in the delay element during the second cycle so it can be synchronized with D for the AND gate to work correctly.

Multi-level Logic with Multiple Outputs

Outputs from logic gates can be used as inputs in more than one place. Broadcasting an output is done easily for conventional transistor logic. The output of a transistor logic gate is statically stable and can be connected to many other gate inputs as long as the combined voltages and currents keep the transistors in the gates in their proper operating modes.

Figure 10 shows an example of a multiple output logic circuit. The set of inputs (A-F) are presented to the OR-gates on level 1. Output H from the middle OR-gate is broadcast to two AND gates at level 2. This broadcast requires no additional circuits in transistor based logic.

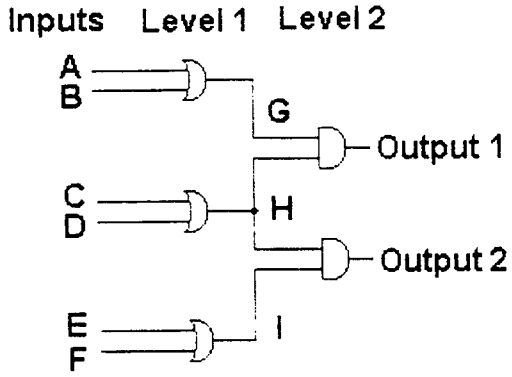

Figure 10. Multi-Level Multiple Output Circuit.

But for quantum logic, it is not as simple. Several connections to an output could cause the quantum gate to work incorrectly. Therefore, we solve this problem by adding delay elements. We use them to generate multiple outputs, by taking in a single signal and being able to copy it to two outputs. Mozyrsky [24] and Buzek and Hillery [8] have suggested some forms of quantum copying, and these are different from the technique suggested here.

Figure 11 shows the implementation of the multiple output circuit using quantum devices. In order to implement the two-way broadcast, a level of delay elements has to be added to distribute the output of the middle OR-gate, and keep the signals synchronized. Larger broadcasts can be done with more levels of delays.

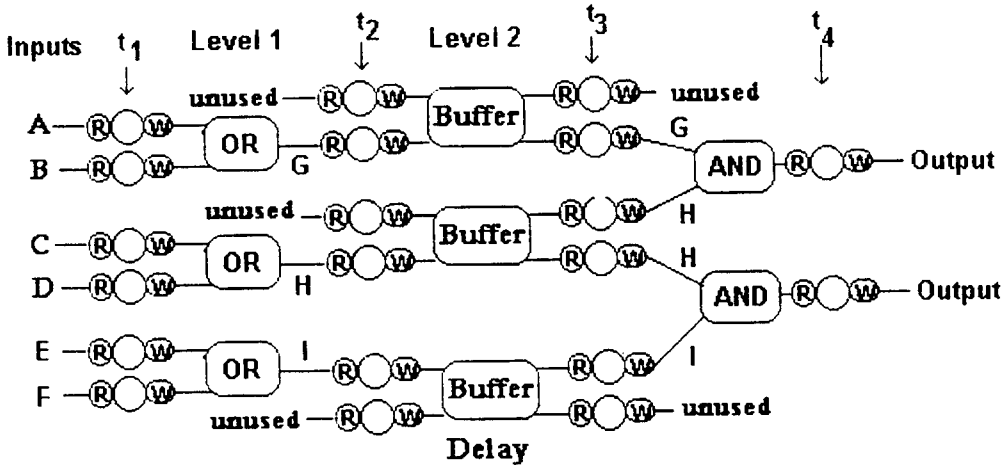

Figure 11. Quantum Implementation of Multi-Level Multiple Output Circuit

Broadcasting leads to another potential problem. The quantum mechanical analog of a *race condition* is potentially possible in the circuit shown in Figure 11. A race condition occurs in conventional systems when two points are switched at the same time and the result is dependant on which finishes last. If one of the output reader/writers is faster than the other, it would read the value in the delay element and that read would corrupt the value so the slower reader/writer would read an incorrect value. The author believes that since reader/writers are activated synchronously, and that they will not have significant variations in switching times that this will not be a problem for quantum circuits.

Bistable Quantum Memory

Conventional memory is implemented using feedback and fact that outputs remain stable after they have switched. A conventional static memory is called a latch or flip-flop and has an output that can remain at zero or one even when the control inputs have been removed. An example is show in Figure 12. Note how the outputs of both NOR gates are fed back to the inputs of the opposite gates.

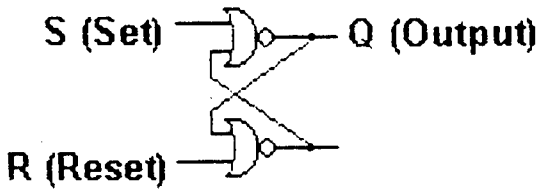

Figure 12. The Conventional Latch, a Basic Bistable Memory Element.

Another form of conventional memory is called Dynamic memory. Information is stored in a capacitive circuit in conventional dynamic memory, with the value decaying over time. Dynamic memory has to be refreshed or periodically re-written to keep the capacitor charged.

Quantum devices are inherently unstable, like capacitors. The idea of using a dynamic structure will be the basis of quantum memory. Quantum memory will be implemented with two delay elements and four reader/writers.

A quantum memory element is shown in Figure 13.

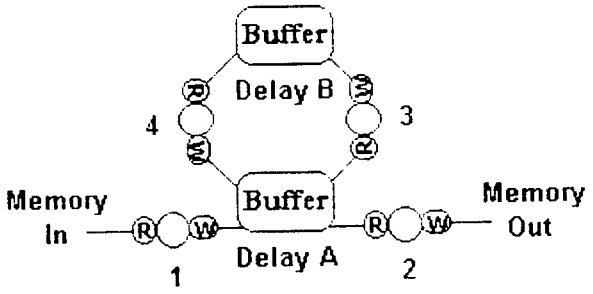

Figure 13. The Quantum Latch, a Dynamically Bistable Memory Element.

To write to memory, reader/writer 1 on the memory input is activated. This stores the value in delay element A. Then, in a systolic manner, reader/writer 3 is activated to read delay A. This is followed by reader/writer 4 reading delay B and writing to delay A. The result is circulated between A and B, continually refreshing the value. Any time reader/writer 3 is activated, reader/writer 2 can be activated to read the value in memory. This is the only time the memory can be read without destroying the value. The resultant circuit will be called the Quantum Latch.

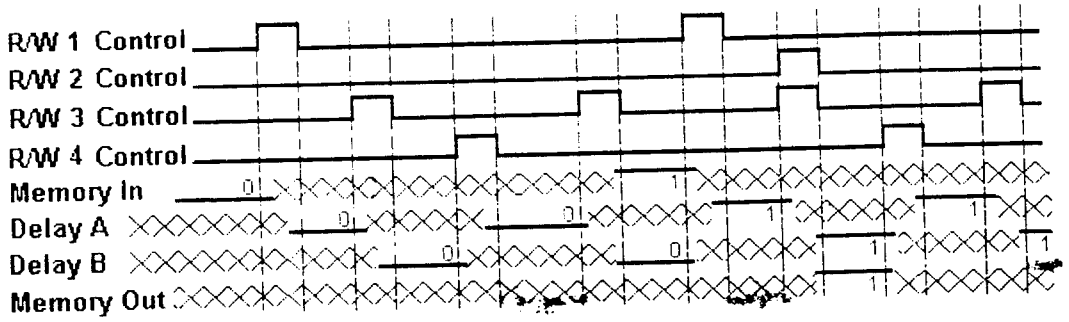

Figure 14. Timing Diagram for the Quantum Latch.

The timing diagram showing the dynamic storage capability of the quantum latch is shown in Figure 14. The external memory input to the latch (reader/writer 1) receives a value in the first

(0) and fifth (1) cycles, and then that input is stored in delay A. Note the stored value reappears every two cycles in Delay A until it is changed. The only time it is read on the output is when reader/writer 2 is pulsed, and in the seventh cycle the stored one is read, but the values in the memory remain.

Quantum Synchronous Sequential Circuits

All synchronous logic system are based on one of four types of storage devices:

RS Flip Flop, the Reset Set Flip-Flop that has an indeterminate state for one possible input combination, and this makes it least desirable to use.

D Flip-Flop, the Delay flip-flop which stores data at its input.

T Flip-Flop, the Toggle flip-flop which changes its output when a one is put on its input. (Used in counters.)

JK Flip-Flop, the JK flip-flop is used for most sequential machine design because it minimizes the number of logic gates required to control it.

All of these flip-flops are clocked and their outputs change based on their being clocked. Thus, they have synchronous operation. All flip-flops have an output called Q. For all flip flops Q and Q' (the compliment of Q) are available. The RS is not used in most designs because it has the race condition mentioned before. Quantum circuits can be used to implement the D, T and JK flip-flops.

Quantum D Flip flop

The D flip-flop has the following characteristic equation:

$$Q^+ = D$$

Where Q^+ is the next state of the flip-flop and D is the input.

The quantum latch has some circuits added on the output to give both Q and Q'. These are necessary to copy the result and then invert it. This is done synchronously, but slows the effective speed of the availability of results by two cycles.

The quantum D flip-flop is shown in Figure 15.

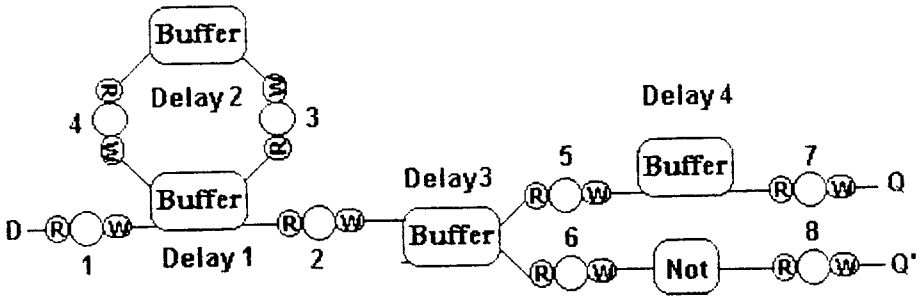

Figure 15. Quantum D Flip-Flop.

The quantum D flip-flop has an input reader/writer 1, with the input D. The buffer in Delay 3 takes the stored value to the output and makes a copy of it so it can be inverted for Q'. The other copy is sent through Delay 4 and becomes Q.

This circuit has a timing diagram shown in Figure 16. Note that there is a delay before both Q and Q' are available, and these values are only correct every two cycles, but that is consistent with all of the other circuits. The input on D is available in cycles 1 and 5. They appear on Q and Q' on cycles 5 and 9. Thus the four cycle delay until the stored value is at Q. Note that it remains at Q in cycle 7 and doesn't change until cycle 9, synchronously with the inputs.

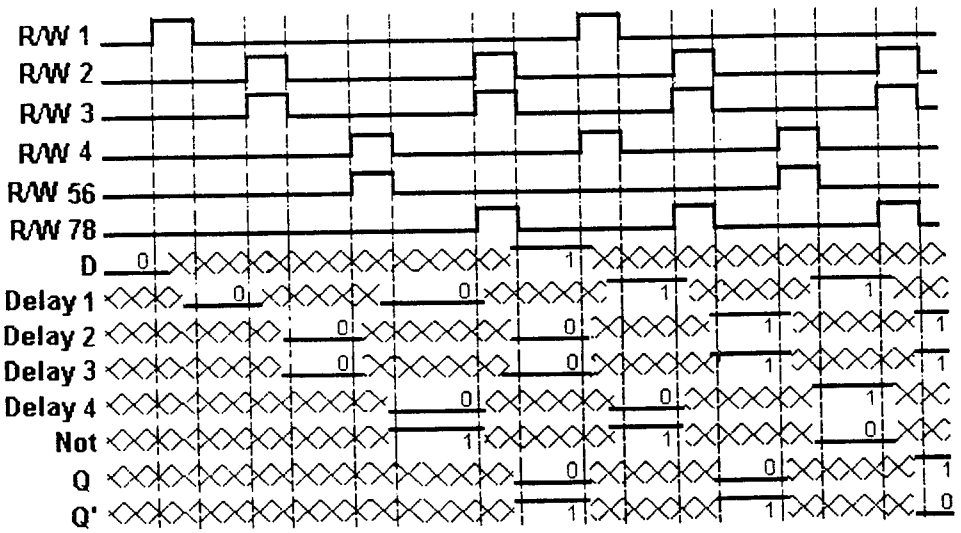

Figure 16. Timing Diagram for the Quantum D Flip-Flop.

There is another important input needed in a flip-flop used for sequential system design. That is an input for asynchronous presetting of the Q value. It is used to initialize the value stored. The circuit for the D flip-flop with a Preset/Clear is shown in Figure 17. The present value (1) or clear value (0) is placed on the preset input and the reader/writer for that input is activated. The input value for the other input reader/writer is not activated. These inputs to the Delay gate are operated mutually exclusively, to insure that a valid 0 is put at the output of the gate when clearing the flip-flop.

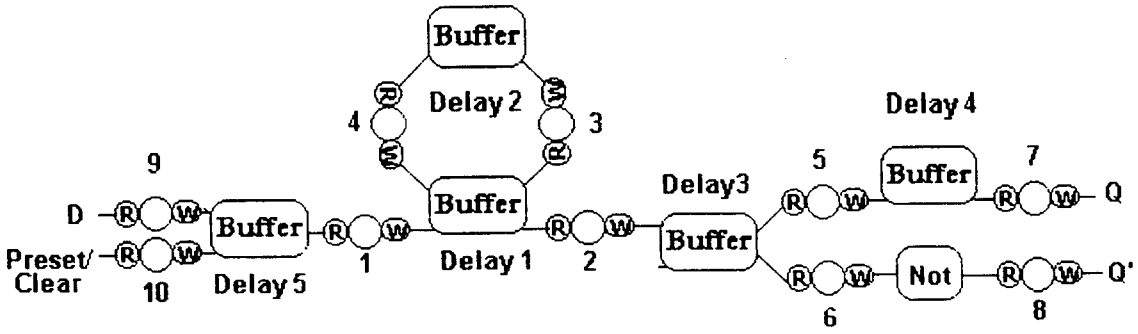

Figure 17. Quantum D Flip-Flop with Preset/Clear.

Quantum T Flip-Flop

The T flip-flop has the following characteristic equation:

$$Q^+ = T\,Q'$$

Where Q^+ is the next state of the flip-flop output, Q is the present state of the flip-flop output, and T is the input. (' indicates not.)

The quantum latch has some circuits added on the outputs to give both Q and Q', and some circuits on the input to provide the toggle control. The extra circuits on the input implement feedback of the present value stored in the flip-flop so it can be combined with the T input to change the stored value when T is one, and not changed when T is zero.

The quantum T flip-flop is shown in Figure 18.

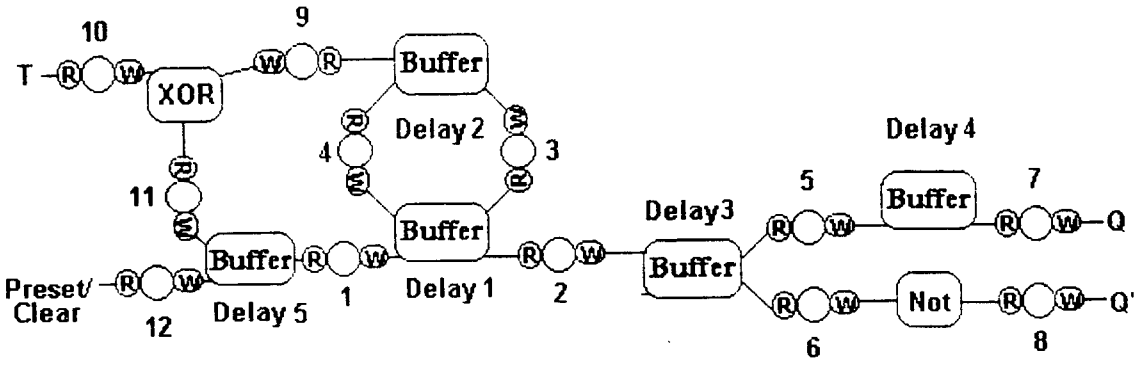

Figure 18. Quantum T Flip-Flop.

The quantum T flip-flop has a timing diagram shown in Figure 19. Note that there is a delay of four cycles before both Q and Q' are available. Inputs of 1 are put on T at cycles 1 and 5. The results on Q then change at cycles 5 and 9. Q and Q' values are only correct every two cycles, but that is consistent with all of the other circuits.

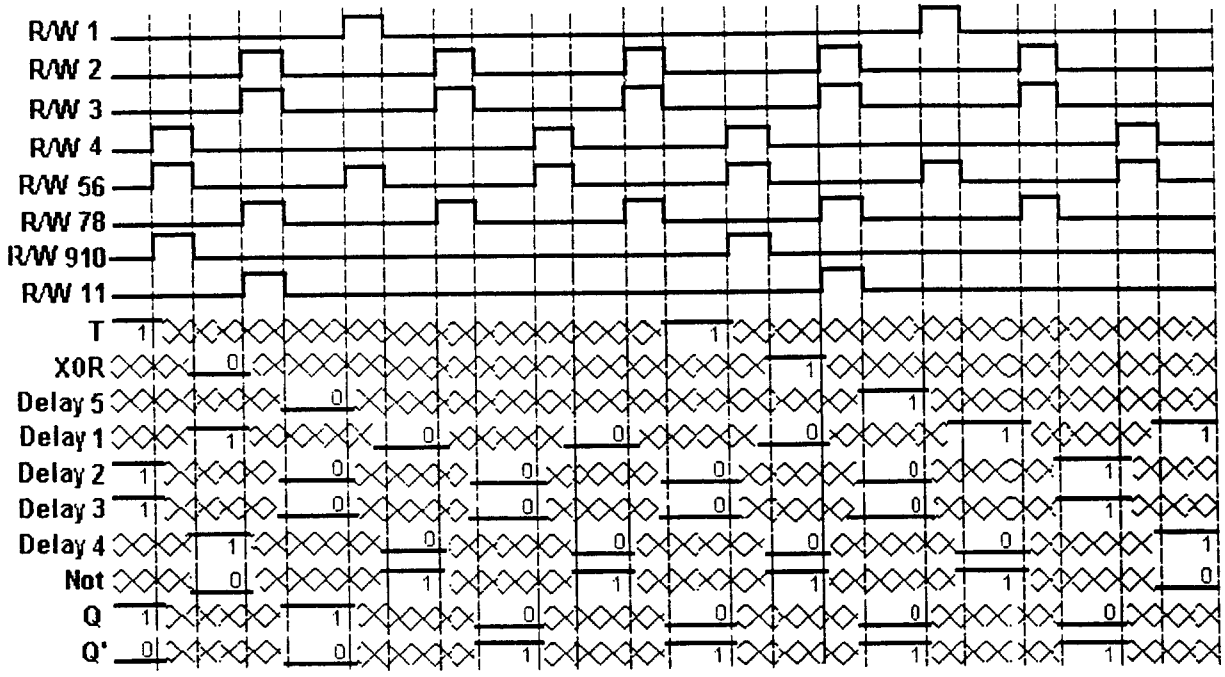

Figure 19. Timing Diagram for the Quantum T Flip-Flop.

Quantum JK Flip-Flop

The JK flip-flop has the following characteristic equation:

$$Q^+ = J\,Q' + K'Q$$

Where Q^+ is the next state of the flip-flop output, Q is the present state of the flip-flop output, and J and K are the inputs. (' indicates not.)

The quantum latch has some circuits added on the outputs to give both Q and Q', and two sets of logic circuits on the input to provide the two possible control states given by the J and K inputs. The quantum JK flip-flop is shown in Figure 20.

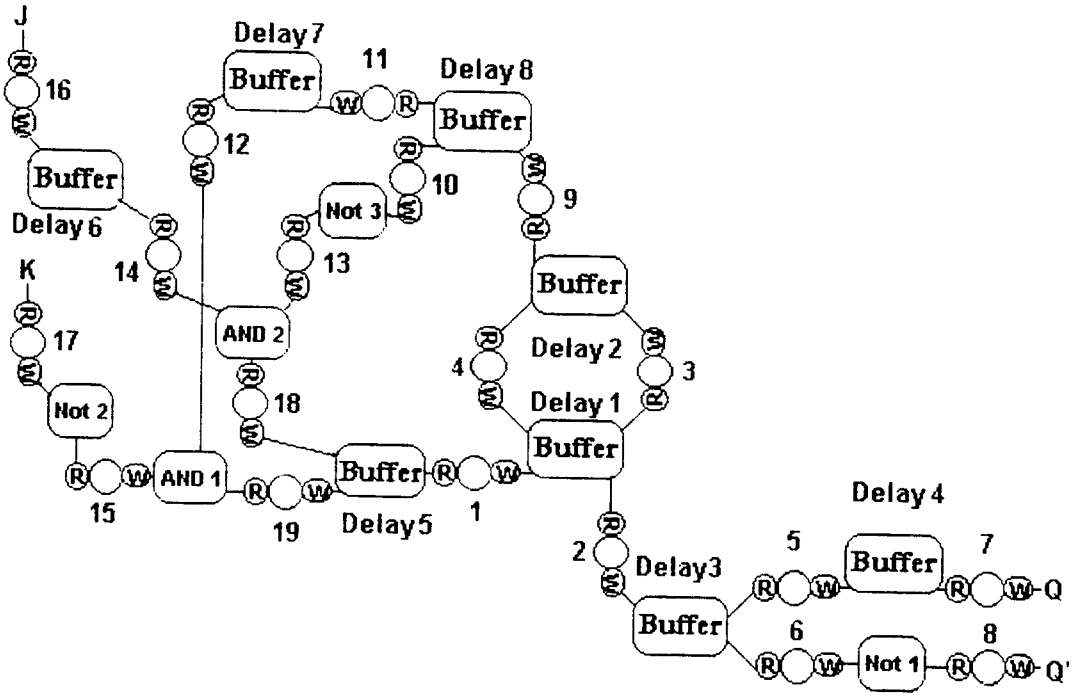

Figure 20. Quantum JK Flip-Flop.

The quantum JK flip-flop circuit has a timing diagram shown in Figure 21. Inputs on J and K are set on cycles 1 and 7. The results of these inputs are then seen to change Q on cycles 7 and 13. Note that there is a 6 cycle delay before both Q and Q' are available. The Q and Q' values are only correct every two cycles, but that is consistent with all of the other circuits.

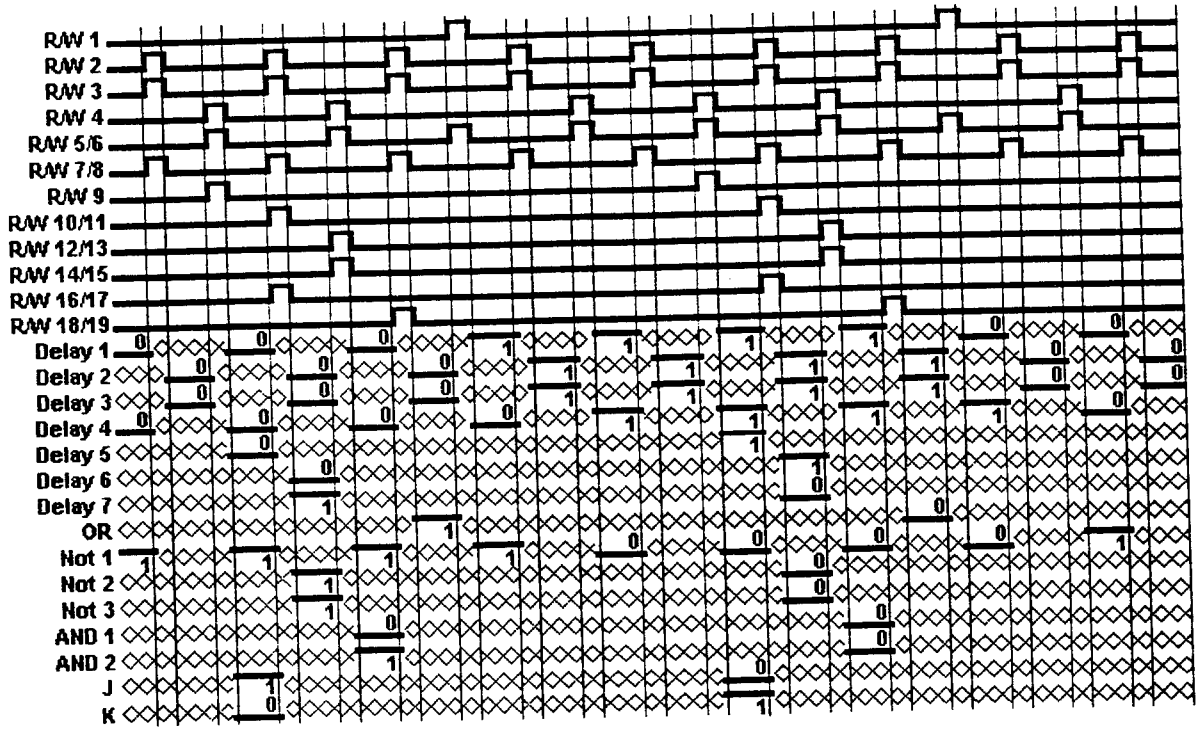

Figure 21. Timing Diagram for the Quantum JK Flip Flop.

Quantum Majority Logic - Reliable Operation Through Redundancy

Three bit quantum logic gates have been suggested by Cory [12]. An interesting 3-input logic gate could then provide more reliable operation of quantum logic by correcting single errors.

The following truth table for a three input, (A,B,C) majority [19] logic gate with output D:

A	B	C	D
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

This is called a majority gate and if used with three redundant copies of quantum logic would correct an error in any one of the three copies of the circuit. This connection scheme is shown in Figure 22.

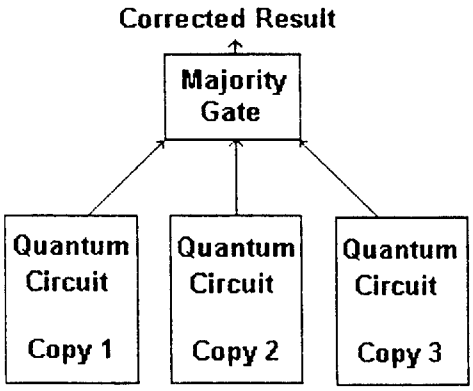

Figure 22. Using the Universal Quantum Logic Gate as a Majority Logic Gate.

Taking this majority logic gate and connecting it to three redundant systems of quantum logic gates, will take the three outputs and combine them into a single result. In the process, the majority logic gate will correct a single error. This is shown in Figure 22. By inserting this at all key outputs and using redundancy, the quantum circuits will be significantly more reliable.

Conclusion

Quantum devices can implement all of the fundamental components that are the basis of combinatorial and sequential machine design. The combinatorial circuits which are asynchronous in conventional logic will have to be synchronous in quantum logic. The flip-flop that offers the best performance for quantum memory is the quantum D flip-flop. It has the smallest delay and contains the fewest parts.

Redundancy can be used and taken advantage of using quantum majority logic. Therefore, the transition from existing system designs based on transistor logic to quantum logic will be feasible. The fundamental difference will be that even at a low level all quantum devices will have to be run synchronously.

Future work that is planned is:

1. Investigating in more detail the feasibility of the reader/writer.
2. Determining if more complicated circuits can be constructed with the results of this paper.
3. The dynamic operation of quantum memory and combinatorial circuits suggest that they may best be modeled with Petri-Nets or some other synchronous modeling technique.

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